In the Specification:

Please replace the section under the heading "BRIEF DESCRIPTION OF THE DRAWINGS" (as already amended in Amendment A) located on pages 4 and 5 of the original specification with the following:

Figure 1 is a circuit diagram of a clocked flip-flop for illustrating setup/hold time violations;

Figure 2 is a circuit diagram illustrating the signal-time curves in the flip-flop according to Figure 1 in which no unknown statusses occur;

Figure 3 is a circuit diagram illustrating the signal-time curves in the flip-flop according to Figure 1, in which unknown statusses occur;

Figure 4 is a block circuit diagram of a clocked circuit with asynchronous signals;

Figure 5 is a block circuit diagram of a circuit for illustrating the conversion into a hardware description language;

Figure 6 is a diagram illustrating the inventively generated network list for the circuit according to Figure 5;

Figure 7 is a diagram illustrating the network list of a further exemplary embodiment for the imaginary flip-flop according to Figure 6;

Figure 8 is a block circuit diagram with a logic causing a setup-time violation;

Figure 9 is a timing diagram illustrating the signal-time curves of the circuit according to Figure 6; ~~and~~

Figure 10 is a timing diagram illustrating the signal-time curves of the circuit according to ~~Figure 8.~~ Figure 8;

Figure 11 is a flowchart of a method in accordance with the present invention; and

Figure 12 is an apparatus implementing a method in accordance with the present invention.